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ABSTRACT OF THE DISCLOSURE

An arrangement for generating addresses for interleaving/de-interleaving sequences ($X_1, X_2, X_3, \dots, X_K$) including a given number (K) of items, wherein each value for said given number (K) identifies a corresponding set of interleaving parameters (R, C, p, v). The arrangement has at least one memory unit wherein a plurality of records are stored, each record being indicative of a respective set of parameters (R, C, p, v) corresponding to at least one value for said given number (K). Sets of interleaving parameters (R, C, p, v) are thus available in the memory unit to be promptly and directly retrieved for all possible values of said given number of items (K). A preferred use is in turbo encoders/decoders for advanced telecommunications applications such as UMTS.